

Notice of References Cited	Application/Control No. 10/827,360	Applicant(s)/Patent Under Reexamination PHELPS ET AL.	
	Examiner Thomas J. Cleary	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,925,118	07-1999	Revilla et al.	710/110
	B	US-5,920,894	07-1999	Plog et al.	711/151
	C	US-5,128,926	07-1992	Perlman et al.	370/248
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kim et al. "Hardware Synthesis for Stack type Partitioned-Bus Architecture". Institute of Electrical and Electronics Engineers. 1999. CD5-01. 0-7803-5727-2/99.
	V	Ewering. "Automatic High Level Synthesis of Partitioned Busses". Institute of Electrical and Electronics Engineers. 1990. CH2924-9/90/0000/0304.
	W	Frank et al. "Constrained Register Allocation in Bus Architectures". Association for Computing Machinery. 1995. 32nd ACM/IEEE Design Automation Conference. 0-89791-756-1/95/0006.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.